Super Linear Headphone Amplifier

XEN Audio

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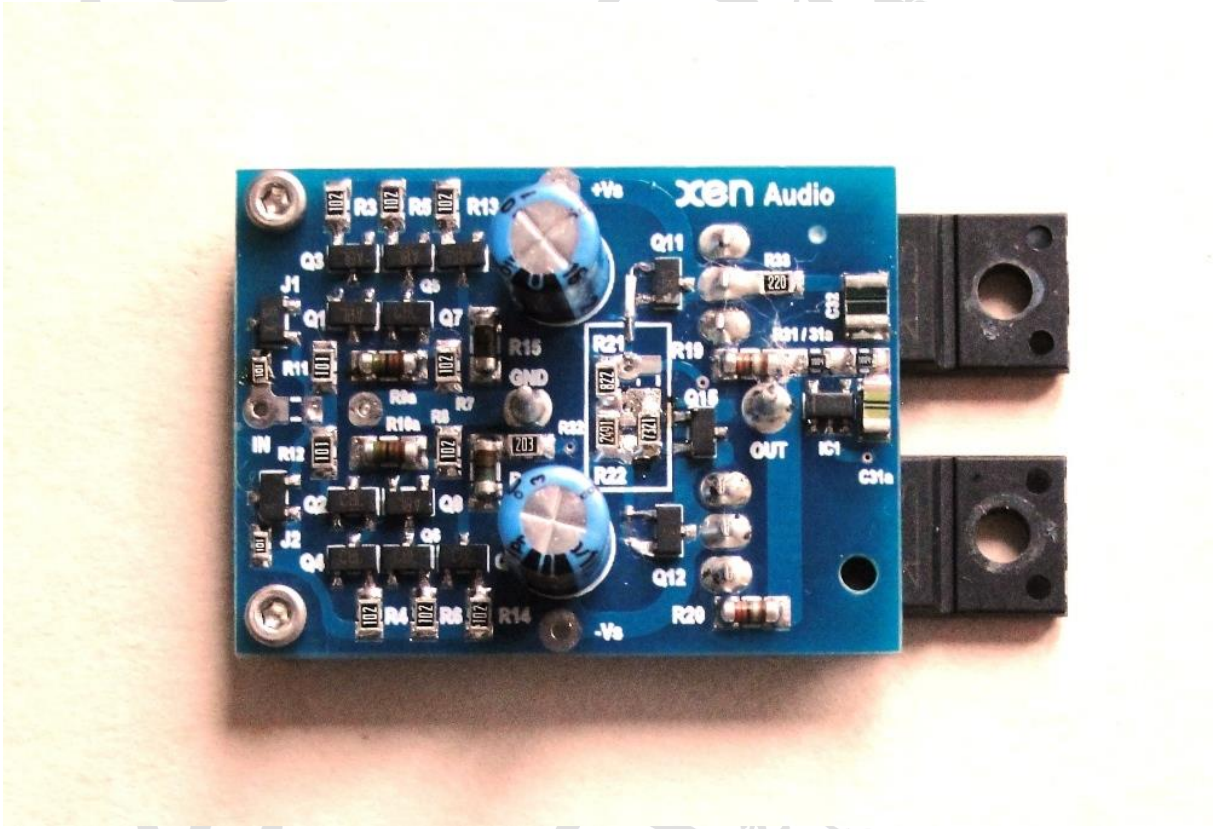


Background

In 1980, Pioneer developed and published a circuit they called Super Linear Circuit [1] , which they subsequently used in their products through to the 90's [2]. Notably, the voltage gain stages were implemented with no global negative feedback but still had very low distortion.

Many descriptions of the circuit can be found on Japanese sites, and there are some disputes as to its origin [3, 4]. A good description in English can also be found in Ref. 5.

The circuit makes use of the fact that NPN and PNP BJTs are almost truly complementary, and hence the non-linear Ic vs. Vbe variation will cancel when the devices have the same hfe and Vbe. Actually in that sense not unlike a diamond buffer. The intelligent bit is that this can produce gain by setting 2 resistor values, without global NFB. If you believe in simulations, then the performance is actually excellent. But as already mentioned, it requires hfe and Vbe matching for best performances. Still, this is a lot simpler than matching JFETs. And as in all BJT design, input impedance is not great, and there can be quite some input bias current (~1µA). So a low impedance driving source is required.

A version of this circuit has been built and published by Andrea Ciuffoli as a headphone amplifier, and some other examples have been built successfully [6, 7, 8]. This is essentially the same circuit as Fig. 17 & Fig. 29 of Ref. 1, and consists of a complementary gain stage as in Figure 1, followed by a complementary Darlington emitter follower. The biasing circuit for the Darlington is a simple (trimmer) resistor in parallel with a capacitor. Due to the fact that the Vbe of a bipolar transistor has a negative tempco, there was fear of thermal run-away of the output stage, so the recommended bias was limited

to 70mA. A DC servo was also included and connected to the input, which also include an input coupling cap to block off any DC from the source.

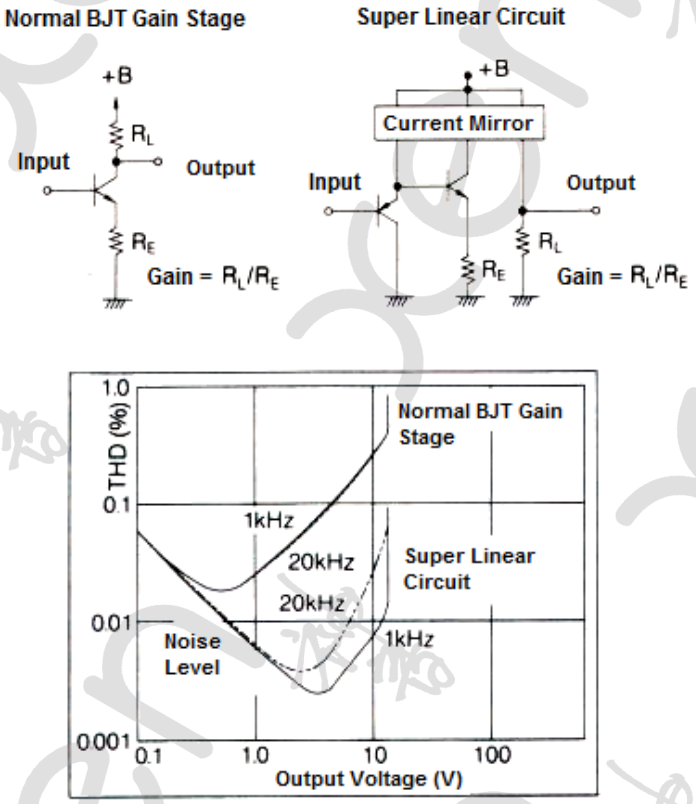


Fig. 1 Pioneer Super Linear Circuit

Although we are known for building FET circuits, this circuit is actually quite interesting. It is nice and symmetrical, does not use any expensive or difficult-to-get components, and can be built even without any matching (with some performance penalties). We set out to build a couple of examples using Toshiba and Sanken transistors, but you can equally well use NXP or On Semi alternatives. The basic circuit is shown in Fig. 2.

As can be seen, there are a few minor changes which are nevertheless important. In the circuit shown, the bias of the top and bottom half of the front end is determined by –Vs / (R9+R9a) and +Vs / (R10+R10a) respectively. If the resistors are well matched, and the rail voltages are identical, the DC offset at the output should be zero. However, about 50% of any mismatch in rail voltages (over time) will result in output DC shift. One could of course use stable regulators for the rails, and trim R9 and R10 at steady state for zero DC. But this is one particular case where the advantage of a DC servo outweighs its disadvantages. Adding optionally C9, 10 helps to reduce the effect of power rail noise on the front end bias significantly. The penalty is that the Murata X5R capacitors have a dissipation factor of about 1.5% in the audio band (similarly Panasonic ECPU). And the signal does go through them. So one might choose to skip those and put extra effort on the power supply instead.

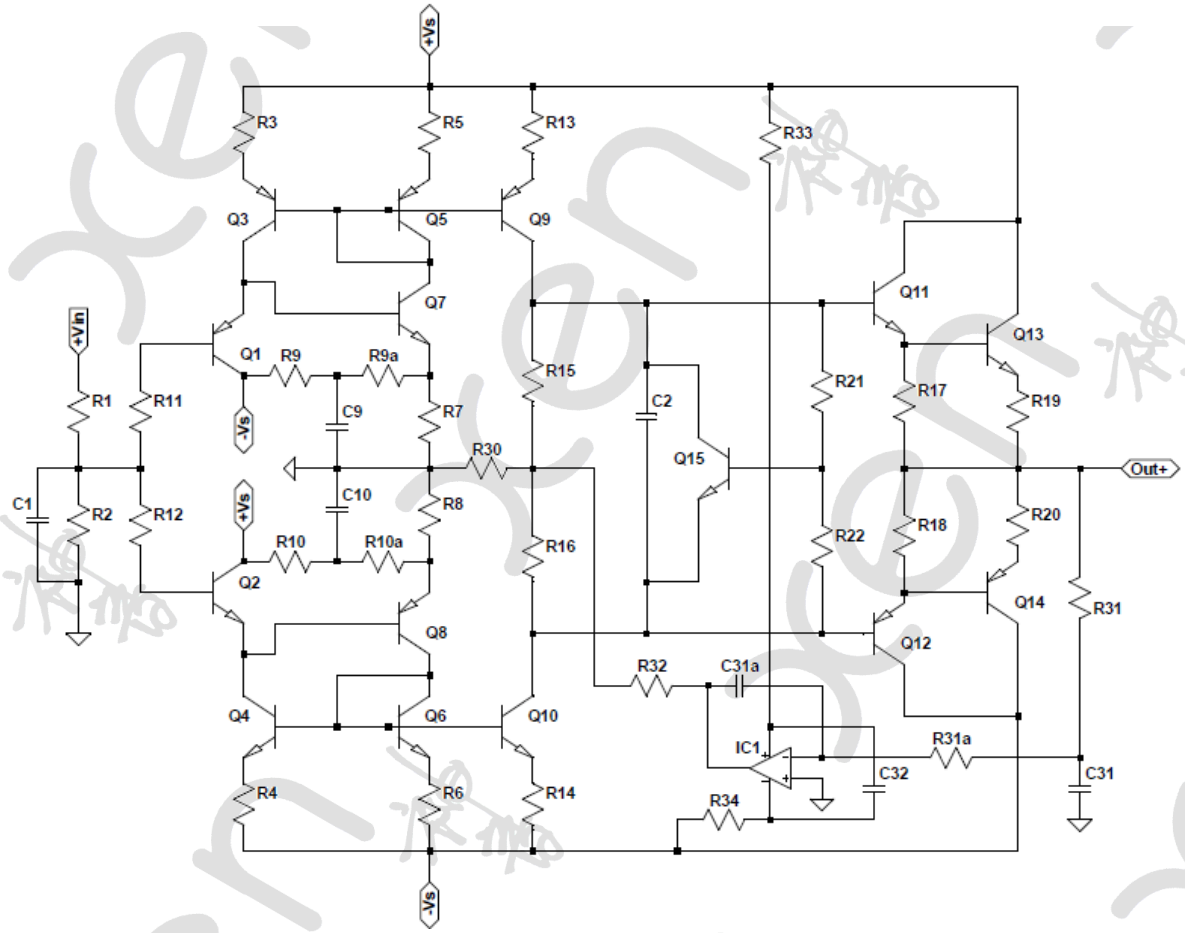


Fig. 2 Super Linear HPA Schematics

With a DC servo, we wanted to avoid then using an input coupling cap. Instead of feeding the servo output to the input, we sacrificed a bit of DC gain and placed the servo at the output biasing circuit instead. This consists of IC1, R30 ~ 34, and C31 ~ 32. One can skip all these components if one prefers resistor trimming (R10) to using a DC servo. The PCB is designed to take care of both.

For bias stability, a common trick is to use a Vbe multiplier instead of fixed resistors. In particular, if the BJT of the Vbe multiplier is made to thermally track the output devices, their Vbe changes with temperature cancels out. When using SOT23 devices, it is rather difficult to place the device directly on top of a TO220 power device. Luckily, the silicon die itself sits directly on the collector lead frame for both devices. By placing the collector pins close to each other, the devices are also thermally coupled. For the Vbe multiplier, it is electrically not feasible to connect the collector to any of the TO220s. So instead a thermal trace is included from Q14 to completely surround the package of Q15, so that the latter essentially sees the same temperature of former.

It was mentioned earlier that the frontend has some similarities to the common diamond buffer. Of course we can equally well hang a diamond buffer at the output of the frontend (at the collectors of Q9. 10 which should then be joined together). This gets rid of the need of the biasing circuit. Provided that the input devices and the drivers of the diamond buffer are coupled thermally, it is also thermally self-compensating. The key disadvantage, apart from requiring 2x current sources, is that the buffer input devices has to see a lot more quiescent current that in the case of the normal emitter follower. After some considerations, it was considered that the disadvantages outweigh the advantage.

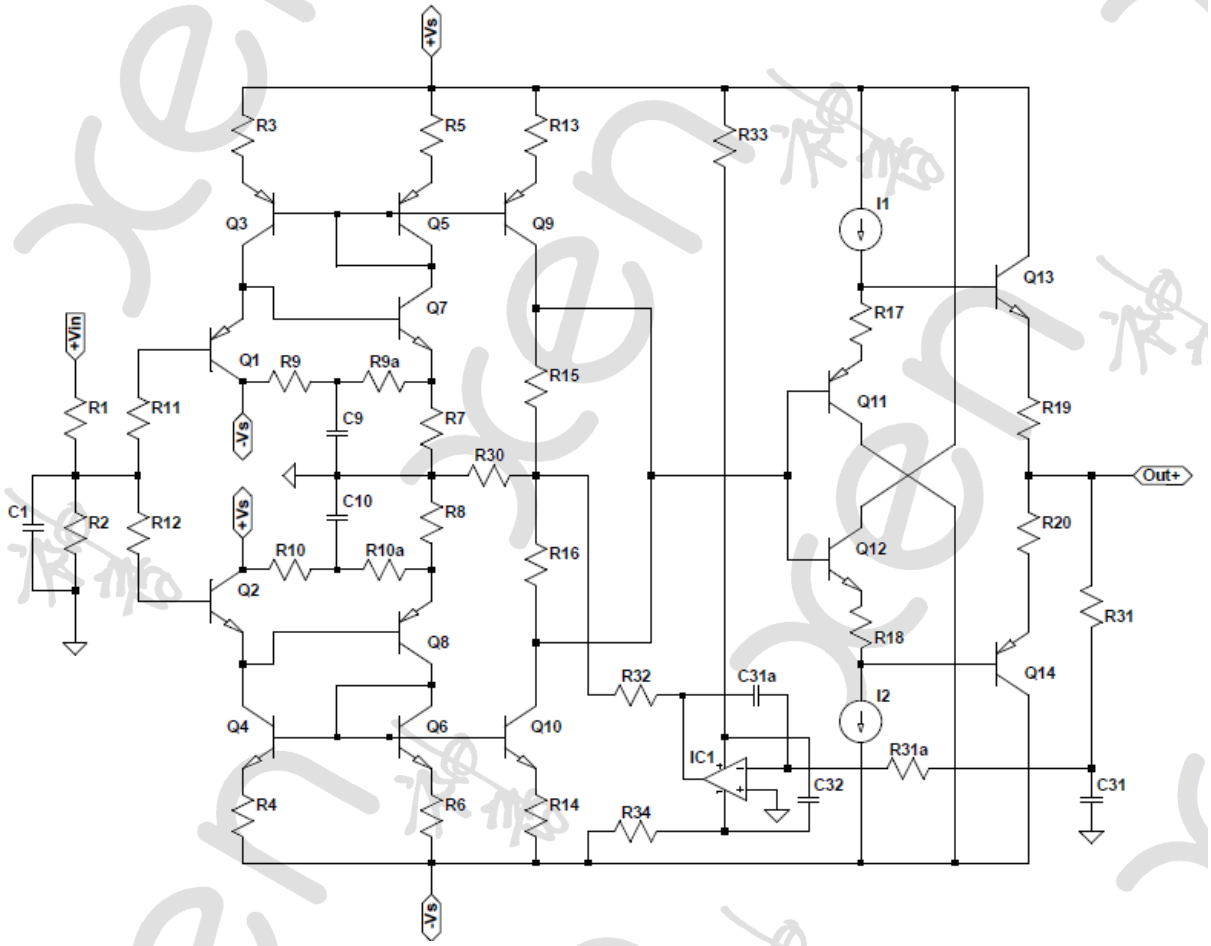


Fig. 3 Super Linear HPA with Diamond Buffer

Since the frontend bias of the super linear circuit is dependent on the rail voltages, it is certainly beneficial to have stable, well-regulated, low-noise rail voltages, e.g. by using the Didden super regulators. In addition, to work around the input impedance of the frontend BJTs, a JFET source follower can be added upstream, as in Fig. 17 of Ref. 1. When using J1,2, R1 and C1 should be left unpopulated.

Actually the circuit is very versatile and not limited to headphones or line amps. In Fig.23 & 24 of Ref. 1, Ozawa demonstrated how this Super Linear circuit can also be applied as a phono preamp with purely passive RIAA equalisation. The low-noise Toshiba transistors chosen are certainly more than adequate for the purpose.

Prototype Measurements

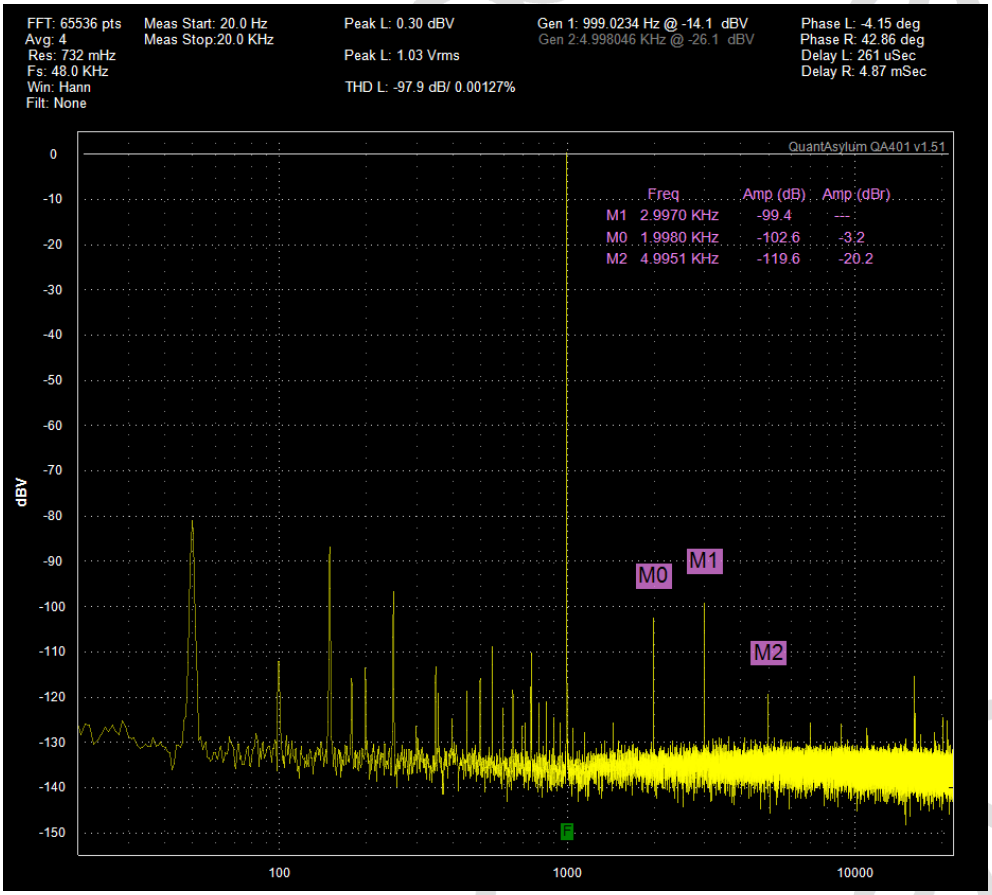
As a proof of principle, a pair of prototypes were built. Small signal transistors were 2SC3324BL / 2SA1312BL, and output transistors were Sanken 2SC24883A / 2SA1859A. All BJTs in complementary positions were hfe matched to better than 1%. The servo and the input JFET buffer were left out initially in order to demonstrate the raw performance of the circuit itself. They were only added later at the end.

Without any trimming, DC offset was less than -60mV on both channels, but this in effect is only 6µA in bias current. The DC offset remains stable with time, as the heatsinks warmed up. The bias

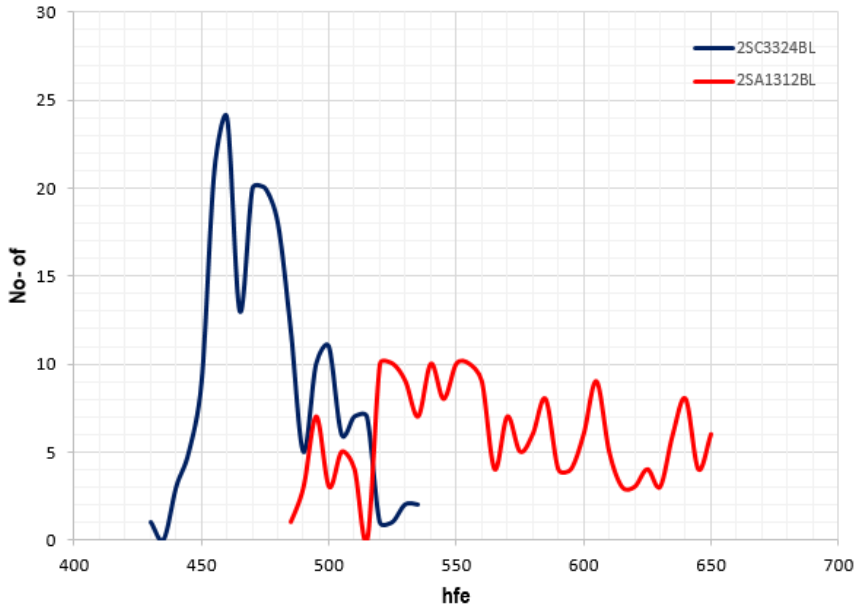
trimmer was not necessary as the simulated values proved to be very accurate. But this might vary for different devices or different degrees of matching. Bias is very stable with temperature and remained 150mA throughout; that means the thermal tracking of the biasing circuit functions as intended.

AC performance was also excellent. -3dB bandwidth is 2MHz, as simulated. 100kHz sine, triangular and square waves were copybook perfect. Maximum output is as much as +/-10V into 30R without clipping !!!

The level of transistor matching manifests itself in the distortion spectrum. With $1V_{rms}$ into 30R load, 2nd harmonics was -103dB, even lower than 3rd at -99dB. 4th was below noise level (-130dB), and 5th was at -120dB. These are excellent results especially for a circuit without any loop feedback throughout. (The noise at mains frequencies came from the lab supply used for the test.)



In the ideal case, all small signal BJTs should have the same hfe and Vbe. In practice, this might be difficult to realise, unless one has a large matching pool. Below is the hfe distribution of 200x of 2SC3324BL and 2SA1312BL ordered from Mouser on tape. It can be seen that the overlap region (for NP match) is relatively small.



For minimising even harmonic distortion, it is important that :

1) Q1, 2, 7, 8 are hfe matched;
2) Q11, 12, are hfe matched, as are Q13, 14;
3) Q3, 5, 9 are hfe matched; as are Q4, 6, 10;

But the hfe between 1), 2) and 3) can be different.

Power Supply Requirements

As already mentioned, the output is quite sensitive to power supply drift, but also power supply noise. This is due to the simple biasing of Q7, 8 using resistors (R9, 9a and R10, 10a). One can improve the PSRR by replacing them with 2x low-drift, low-noise constant-current sources. One of them can then be adjusted to null any DC offset. But this is also easier said than done.

One can of course concentrate the effort on the power supply itself instead, e.g. by using the likes of the Didden super regulators. It is also advantages to use separate power supplies (with same voltage or not) for the Super Linear gain stage and the Darlington follower or diamond buffer.

Yet another alternative is to use a single 30V floating supply connected to +Vs and –Vs directly, e.g. a LM317 pre-reg at 32V output, followed by a TPS7A4700 at 30V, plus a virtual ground circuit capable of the maximum output current (300mA), e.g. using an OPA554 with a pair of 0.1% resistors as potential divider. The advantage of such a solution is that any noise or drift from the 30V power supply is equally shared by the positive and negative rails, which then cancel themselves in the front end circuit.

Other versions

The circuit as shown has a voltage gain of 10. This is designed to be used in combination with the Danyuk cross-feed, which has an attenuation of 3. Should one prefer to use the amplifier without

cross feed, a gain of 3 should be sufficient. In that case, the diamond buffer version is preferred, as it is much simpler to change gain (by changing R15, 16 to 2k) than the Darlington version.

The PCB is also small enough to be used as a portable. Both the voltage and bias current, however, need to be reduced to give reasonable battery life and heat dissipation. Performance is still very decent when using +/-9V rails and 50mA bias. One can then use the Toshiba TTA004B / TTC004B which are smaller in size. Power can then come from batteries, or Jan Didden's USB Silent Switcher.

The reduced bias, together with higher emitter resistors (e.g. 3R) for the output pair, is also useful if one choose to use the Super Linear circuit for other applications where it is only required to drive higher impedances (e.g. > 500R).

References

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Appendix 1 Bill of Materials – Darlington Version (Fig. 2)

Per Channel (+/-15V rails)

Quantity	Designation	Description	Alternatives
5	Q1,3,5,8,9,12	2SA1312BL, matched hfe	BC807-40
5	Q2,4,6,7,10,11	2SC3324BL, matched hfe to the above	BC817-40
1	Q13	2SC4883	D44H11
1	Q14	2SA1859, matched hfe to Q13	D45H11
1	Q15	2SC3324BL	BC817-40
1	IC1	OPA140, SOT23-5	LT1880
1	R1 11, 12	Susumu 0805 100R 0.5%	skip R1 for J1,2
1	R2,	Susumu 0805 100k 0.5%	skip R2 for J1,2
8	R3~8, 13, 14	Susumu 0805 1k 0.1%	
2	R9, 10	Susumu 0805 5.1k 0.1%	Trim DC offset
2	R9a, 10a	Beyschlag MMA0204 5.1k 0.1%	
2	R15, 16	Beyschlag MMA0204 6.2k 0.1%	
2	R17, 18	Susumu 0805 1k 0.5%	
2	R19, 20	Beyschlag MMA0204 1R 0.5%	
--	R21, 22	Use 10k trimmer to set bias Then replace with 0805 fixed resistors	
1 -	R30	Susumu 0805 2k 0.1%	
2	R31, R31a	Susumu 0805 1M 1%	
1	R32	Susumu 0805 20k 0.5%	
2	R33, 34	Susumu 0805 22R 0.5%	
1	C1	0805 100p (optional)	skip for J1,2
1	C2	Panasonic 1210 ECPU 16V 20% 1µ	
2	C3, 4	Panasonic 0805 ECPU 16V 20% 100n	
2	C6, 7	Nichicon KA 220µ 16V	
2	C9, 10	Murata 1210 X5R 16V 10% 47µ	optional
1	C31	Panasonic 0805 ECPU 16V 20% 100n	
1	C31a	Panasonic 1206 ECPU 16V 20% 680n	
1	C32	Panasonic 1210 ECHU 50V 5% 33n	WIMA MKS02 1 µ

Not shown in schematics

2	J1,2	2SK209GR, matched Idss	
2	Rg1,2	Susumu 0603 100R 0.5%	
1	R2a	Susumu 0805 100k 0.5%	only with J1,2

Note :
When not using DC servo, omit IC1, R31 ~ 34, C31 ~ 32. Trim DC offset using R10.
When using (optional) J1,2 as input, R1, C1 must be left unpopulated.